III-NITRIDE SEMICONDUCTOR LIGHT EMITTING DEVICE

[0001] Technical Field

[0002] The present invention relates to a III-nitride semiconductor light emitting device, and more particularly, to a III-nitride semiconductor light emitting device in which contact resistance between a p-type nitride semiconductor layer and a p-side electrode adjacent to the p-type nitride semiconductor layer is reduced and holes are thus effectively supplied to an active layer. In this case, the III-nitride semiconductor light emitting device refers to a light emitting device such as a light emitting diode including an Al(x)Ga(y)In(1-x-y)N ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x+y \leq 1$) compound semiconductor layer, but does not exclude semiconductor layers or materials made of elements of different groups, such as SiC, SiN, SiCN and CN.

[0003] [Background Art]

[0004] FIG. 1 is a cross-sectional view illustrating the structure of a III-nitride semiconductor light emitting device in the prior art. The light emitting device includes a substrate 100, a buffer layer 200 epitaxially grown on the substrate 100, an n-type nitride semiconductor layer 300 epitaxially grown on the buffer layer 200, an active layer 400 epitaxially grown on the n-type nitride semiconductor layer 300, a p-type nitride semiconductor layer 500 epitaxially grown on the active layer 400, a p-side electrode 600 formed on the p-type nitride semiconductor layer 500, a p-side bonding pad 700 formed on the p-side electrode 600, and an n-side electrode 800 formed on an n-type nitride semiconductor layer 301 which is exposed by mesa-etching at least the p-type nitride semiconductor layer 500 and the active layer 400.

[0005] The substrate 100 can use a GaN-based substrate as a homogeneous substrate, and a sapphire substrate, a silicon carbide substrate or a silicon substrate as a heterogeneous substrate, but can use any other substrates on which nitride semiconductor layers can be grown.

If the silicon carbide substrate is used, the n-side electrode 800 can be formed on the opposite side of the silicon carbide substrate.

[0006] The nitride semiconductor layers epitaxially grown on the substrate 100 are usually grown by means of MOCVD (Metal Organic Chemical Vapor Deposition) method.

[0007] The buffer layer 200 serves to reduce differences in lattice constant and the coefficient of thermal expansion between the heterogeneous substrate 100 and the nitride semiconductor. U.S. Patent No.5,122,845 discloses a technology in which an AlN buffer layer having a thickness of 100Å to 500Å is grown on a sapphire substrate at a temperature ranging from 380°C to 800°C. U.S. Patent No.5,290,393 discloses a technology in which an Al(x)Ga(1-x)N ($0 \leq x < 1$) buffer layer having a thickness of 10Å to 5000Å is grown on a sapphire substrate at a temperature ranging from 200°C to 900°C. Korean Patent No.10-0448352 discloses a technology in which a SiC buffer layer is grown at a temperature ranging from 600°C to 990°C, and an In(x)Ga(1-x)N ($0 < x \leq 1$) layer is grown on the SiC buffer layer.

[0008] In the n-type nitride semiconductor layer 300, at least a region (n-type contact layer) in which the n-side electrode 800 is formed is doped with an impurity. The n-type contact layer is preferably made of GaN and is doped with Si. U.S. Patent No.5,733,796 discloses a technology in which an n-type contact layer is doped with a desired doping concentration by controlling a mixing ratio of Si and other source materials.

[0009] The active layer 400 is a layer for emitting a photon (light) by recombination of electrons and holes, and is mainly made of In(x)Ga(1-x)N ($0 < x \leq 1$). The active layer 400 is composed of a single quantum well or multi quantum wells. WO02/021121 discloses a technology in which only some of a plurality of quantum wells and barrier layers are doped.

[0010] The p-type nitride semiconductor layer 500 is doped with an impurity such as Mg, and has a p-type conductivity through an activation process. U.S. Patent No.5,247,533 discloses a technology in which a p-type nitride semiconductor layer is activated by means of

irradiation of electron beam. U.S. Patent No.5,306,662 discloses a technology in which a p-type nitride semiconductor layer is activated through annealing at a temperature of 400°C or more. Korean Patent No.10-043346 discloses a technology in which NH_3 and a hydrazine-based source material are used together as a nitrogen precursor for growing a p-type nitride semiconductor layer, so that the p-type nitride semiconductor layer has a p-type conductivity without an activation process.

[0011] The p-side electrode 600 serves to allow the current to be supplied to the entire p-type nitride semiconductor layer 500. U.S. Patent No.5,563,422 discloses a technology of a light-transmitting electrode, which is formed almost on the entire p-type nitride semiconductor layer, in ohmic contact with the p-type nitride semiconductor layer, and made of Ni and Au. Meanwhile, the p-side electrode 600 can be formed to have such a thick thickness that the p-side electrode 600 does not transmit light, i.e., the p-side electrode 600 reflects light toward the substrate. A light emitting device using this p-side electrode 600 is called a flip chip. U.S. Patent No.6,194,743 discloses a technology of an electrode structure including an Ag layer of 20nm or more in thickness, a diffusion barrier layer covering the Ag layer, and a bonding layer made of Au and Al, which covers the diffusion barrier layer.

[0012] In the III-nitride semiconductor light emitting device, the efficiency of a device can be defined as the ratio of the intensity of light generated to external input power. The p-type GaN constituting the p-type nitride semiconductor layer 500 is not good because it has a higher energy bandgap (~3.3eV) and a doping efficiency of below $5x10^{17}atoms/cm^3$. Further, contact resistance between the p-type nitride semiconductor layer 500 and the p-side electrode 600 adjacent to the p-type nitride semiconductor layer 500 is very high. Accordingly, not only the efficiency of a device is not good, but also a higher voltage is needed in order to have the same intensity of light.

[0013] In order to reduce the contact resistance between the p-type nitride semiconductor layer 500 and the p-side electrode 600, p-type GaN doped with a high concentration must be formed. It is, however, very difficult to form p-type GaN doped with a high concentration because of a great bandgap and a low doping efficiency($< 5x10^{17}$atoms/cm^3) of the p-type GaN.

[0014] A variety of methods have been proposed in order to reduce the contact resistance between the p-type GaN used as the p-type nitride semiconductor layer 500 and the p-side electrode 600. Among them, there is a method in which the p-type nitride semiconductor layer 500 is not made of a single p-type GaN layer, but is formed to have a superlattice structure of p-type GaN/p-type InGaN or p-type GaN/p-type AlGaN, and the concentration of holes, which is significantly higher than the concentration that can be obtained in the single p-type GaN layer, is thus obtained within the superlattice structure through piezoelectric field. This method, however, is not preferred that potential barrier is formed in a vertical direction within the superlattice structure before holes are injected into the active layer.

[0015] As another example, there is a method in which a GaAs layer or an AlGaAs layer is grown, which can be doped with a high concentration ($>10^{20}$ atoms/cm^3), between the p-type nitride semiconductor layer 500 and the p-side electrode 600 (U.S. Patent No.6,410,944). In this method, however, since the bandgap of the GaAs layer or the AlGaAs layer is smaller than that of the visible region. Most of light generated from the active layer 400 may be absorbed by the GaAs layer or the AlGaAs layer. Therefore, this method has limited application fields.

[0016] As described above, the conventional III-nitride semiconductor light emitting device is disadvantageous in that the efficiency is low because the contact resistance between the p-type nitride semiconductor layer 500 and the p-side electrode 600 is high. In this connection, there is a need for effective means for overcoming this problem.

DISCLOSURE

[0017] Technical Problem

[0018] Accordingly, the present invention has been made in view of the above problems occurring in the prior art, and it is an object of the present invention to provide a III-nitride semiconductor light emitting device having improved efficiency, in which contact resistance between a p-type nitride semiconductor layer and a p-side electrode formed on the p-type nitride semiconductor layer is reduced.

[0019] Technical Solution

[0020] To achieve the above object, according to the present invention, there is provided a III-nitride semiconductor light emitting device, including a plurality of III-nitride semiconductor layers including an active layer emitting light by recombination of electrons and holes, the plurality of III-nitride semiconductor layers having a p-type III-nitride semiconductor layer at the top thereof, an $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer grown on the p-type III-nitride semiconductor layer, the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer having an n-type conductivity and a thickness of 5Å to 500Å for the holes to be injected into the p-type III-nitride semiconductor layer by tunneling, and a p-side electrode formed on the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer.

[0021] In the present invention, the thickness of the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer has a restriction, so that tunneling is efficiently accomplished. Also, when the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer is made of SiC, the degradation of the plurality of III-nitride semiconductor layers caused by decomposition of nitrogen therefrom during the growth of SiC layer is considered in this restriction.

[0022] In addition, according to the present invention, there is provided a III-nitride semiconductor light emitting device, including a plurality of III-nitride semiconductor layers including an active layer emitting light by recombination of electrons and holes, the plurality of III-nitride semiconductor layers having a p-type III-nitride semiconductor layer at the top

thereof, a $Si_aC_bN_c$ ($a\geq0,b>0,c>0$) layer grown on the p-type III-nitride semiconductor layer, and a p-side electrode formed on the $Si_aC_bN_c$ ($a\geq0,b>0,c>0$) layer.

[0023] In the present invention, during the growth of the $Si_aC_bN_c$ ($a\geq0,b>0,c>0$) layer, nitrogen is continuously supplied because the $Si_aC_bN_c$ ($a\geq0,b>0,c>0$) layer includes nitrogen. Thus, the present invention has an additional advantage that the decomposition of nitrogen is prevented by the $Si_aC_bN_c$ ($a\geq0,b>0,c>0$) layer.

[0024] In the present invention, the p-side electrode may be made of nickel and gold. The alloy of nickel and gold is the representative materials used for the p-side light-transmitting electrode of III-nitride semiconductor light emitting device.

[0025] In the present invention, the p-side electrode may be made of ITO(Indium Tin Oxide). Recently, ITO(Indium Tin Oxide) is widely used as a p-side electrode, but it is not easy to make a good ohmic contact with the p-type semiconductor using ITO(Indium Tin Oxide). The problem can be solved by using the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer with a high doping concentration.

[0026] Advantageous Effects

[0027] Generally, in III-nitride semiconductor light emitting devices, if a p-side electrode is formed directly on a p-type nitride semiconductor, high contact resistance is generated due to a high energy bandgap and low doping efficiency of the p-type nitride semiconductor. This makes the efficiency of the device degraded. According to the present invention, however, a $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer which can be doped with a high concentration is intervened between a p-type nitride semiconductor and a p-side electrode. Therefore, the present invention can solve the conventional problem.

DESCRIPTION OF DRAWINGS

[0028] Further objects and advantages of the invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0029] FIG. 1 is a cross-sectional view illustrating the structure of a III-nitride semiconductor light emitting device in the prior art;

[0030] FIG. 2 is a cross-sectional view illustrating the structure of a III-nitride semiconductor light emitting device according to an embodiment of the present invention;

[0031] FIG. 3 is a graph showing X-ray diffraction (XRD) analysis of silicon carbide grown on a sapphire substrate;

[0032] FIG. 4 shows an energy band diagram of a metal/n-type SiC/p-type GaN structure; and

[0033] FIG. 5 shows an energy band diagram for explaining the operational principle of the metal/p-type SiC/p-type GaN structure.

[0034] Mode for Invention

[0035] The present invention will now be described in detail in connection with preferred embodiments with reference to the accompanying drawings.

[0036] FIG. 2 is a cross-sectional view illustrating the structure of a III-nitride semiconductor light emitting device according to an embodiment of the present invention.

[0037] A buffer layer 11, an n-type nitride semiconductor layer 12, an active layer 13, and a p-type nitride semiconductor layer 14 are sequentially grown on a substrate 10. A p-side electrode 15 and a p-side bonding pad 17 are formed over the p-type nitride semiconductor layer 14. An n-side electrode 16 is formed on the n-type nitride semiconductor layer 121, which is exposed by mesa etching.

[0038] Referring to FIG. 2, unlike the prior art, according to the present invention, an n-type or p-type $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer 21 is intervened between the p-type nitride semiconductor layer 14 and the p-side electrode 15.

[0039] $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) includes silicon carbide [$Si_aC_bN_c$ ($a>0,b>0,c=0$)], silicon carbon nitride [$Si_aC_bN_c$ ($a>0,b>0,c>0$)] or carbon nitride [$Si_aC_bN_c$ ($a=0,b>0,c>0$)], which are a group of materials having the similar properties.

[0040] In the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer 21, an n-type dopant such as Si, N, As or P and a p-type dopant such as B or Al can be easily doped at a high concentration of about $1x10^{18}$ to $1x10^{22}$ atoms/cm^3. Thus, the thickness of a potential barrier can be made thin so that holes can easily pass through the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer 21.

[0041] In FIG. 2, silicon carbide [$Si_aC_bN_c$($a>0,b>0,c=0$)] is used as the $Si_aC_bN_c$ ($a\geq0,b>0,c\geq0,a+c>0$) layer 21. The silicon carbide layer 21 can be obtained by allowing silicon and carbon to react to each other in a deposition apparatus. The silicon source material can include SiH_4, Si_2H_6, DTBSi, etc., and the carbon source material can include CBr_4, C_xH_y, etc.

[0042] Generally, the growth temperature of silicon carbide is over 1300°C. If silicon carbide is formed on a nitride semiconductor such as GaN at too high temperature, however, a GaN based device may be damaged when silicon carbide is grown. Therefore, the growth temperature of silicon carbide is preferably 600°C to 1200°C.

[0043] Further, if the thickness of the silicon carbide layer becomes too thick, a tunneling barrier undesirably thickens. It is thus preferred that the thickness of the silicon carbide layer is about 5Å to 500Å. The doping concentration, thickness, and the growth temperature of the silicon carbide layer can be applied to formation of the silicon carbon nitride [$Si_aC_bN_c$ ($a>0,b>0,c>0$)] layer or the carbon nitride [$Si_aC_bN_c$ ($a=0,b>0,c>0$)] layer in the same manner as well as formation of the silicon carbide layer. In this case, NH_3 and/or hydrazine-based source can be mainly used as a nitrogen source material.

[0044] The p-side electrode 15 and the n-side electrode 16 can be made of at least one selected from the group consisting of nickel, gold, silver, chromium, titanium, platinum, palladium, rhodium, iridium, aluminum, tin, ITO(Indium Tin Oxide), indium, tantalum, copper, cobalt, iron, ruthenium, zirconium, tungsten, lanthanum and molybdenum.

[0045] FIG. 3 is a graph showing X-ray diffraction (XRD) analysis of silicon carbide grown on a sapphire substrate. In this case, the growth temperature was 1000°C and the growth rate was 2Å/sec. Further, the thickness of grown silicon carbide was 5000Å for XRD analysis. NH_3 was used as a N source for high concentration n-type doping. At this time, the doping concentration was $4.63x10^{19}$ atoms/cm^3 so that tunneling can occur sufficiently. From FIG. 3, it can be seen that silicon carbide is well grown.

[0046] Table 1 shows electrical characteristics of a device, which is formed by growing silicon carbide of about 20Å in thickness, which is doped with a high concentration, on a common GaN-based light emitting device. At this time, an electrode used was an ITO(Indium Tin Oxide) electrode. From Table 1, it can be seen that a case where a silicon carbide layer is formed has a low formed on p-type GaN without silicon carbide layer.

[0047] TABLE 1

	CONTACT LAYER	Vf@20mA[V]	Vf@10μA[V]	Vr@-10μA[V]
case 1	p-GaN	5.25	2.37	24.1
case 2	SiC/p-GaN	3.65	2.35	25.1

[0048] FIG. 4 shows a schematic energy band diagram when the n-type silicon carbide layer 21 exits between the p-type nitride semiconductor layer 14 and the p-side electrode 15. From FIG. 4, it can be seen that holes can flow into the p-type nitride semiconductor layer 14 in a more efficient manner since the n-type silicon carbide layer 21 doped with a high concentration exists(E_C: Conduction Band Energy, E_V: Valence Band Energy, E_F: Fermi Energy Level).

[0049] FIG. 5 shows a schematic energy band diagram in the case (a) where the p-side electrode 15 is formed on the p-type nitride semiconductor layer 14 and the case (b) where a p-type silicon carbide layer doped with a high concentration exists between the p-type nitride semiconductor layer 14 and the p-side electrode 15. From FIG. 5, it can be seen that holes H can flow into the p-type nitride semiconductor layer 14 in a more efficient manner in the case where there exists the p-type silicon carbide layer doped with the high concentration(E_C: Conduction Band Energy, E_V: Valence Band Energy, E_F: Fermi Energy Level).

[0050] While the present invention has been described with reference to the particular illustrative embodiments, it is not to be restricted by the embodiments but only by the appended claims. It is to be appreciated that those skilled in the art can change or modify the embodiments without departing from the scope and spirit of the present invention.